REMARKS

The application has been carefully reviewed in light of the Office Action dated September 14, 2010. Claims 1, 3 to 7, 20, 22 to 26 and 39 remain pending in the application, of which Claims 1, 20 and 39 are independent. Reconsideration and further examination are respectfully requested.

As an initial matter, it is noted that Applicant filed a Supplemental Preliminary Amendment on September 8, 2010 which has not been considered by the Examiner. The Supplemental Amendment amended the claims pursuant to an interview conducted with the Examiner on September 2, 2010. The Examiner, however, was apparently required to act on the July 15, 2010 Preliminary Amendment and thus, the present Office Action was issued prior to the Examiner considering the amendments and arguments presented in the Supplemental Amendment. In light of the foregoing, it is requested that the claim amendments presented in the Supplemental Amendment not be entered and that the amendments above be entered instead. Here, it is noted that the claim amendments presented above correspond to those presented in the Supplemental Amendment, but are now being presented in response to the rejections included in the present Office Action. The discussion of patentability, however, included in the Supplemental Amendment is maintained by Applicants and is repeated, at least in part, below.

In the Office Action, Claim 39 was rejected under 35 U.S.C. § 101. Without conceding the correctness of the rejection, the preamble of Claim 39 has been amended to include the term "non-transitory". Reconsideration and withdrawal of the § 101 rejection are respectfully requested.

In addition, Claims 1, 3, 7, 20, 22, 26 and 39 were rejected under 35 U.S.C. § 103(a) over U.S. Patent No. 5,488,673 (Katayama) in view of U.S. Patent No. 6,330,075 (Ishikawa), and Claims 4 to 6 and 23 to 25 were rejected under § 103(a) over Katayama in view of Ishikawa and further in view of U.S. Patent No. 6,977,756 (Nakano). Reconsideration and withdrawal of the rejections are respectfully requested.

During the September 2, 2010 interview, the invention was discussed with particular reference to Figure 1. Here, it was pointed out that the various elements of the claims can be seen correspond to the features of Figure 1 as follows:

a) bit connection component = bit connecting circuit 1

b) correction component = adder 2

c) latch component = latch 3

d) quantization component = quantizer 4

e) inverse quantizing component = inverse quantizer 5

f) calculation component = component 6

g) buffer = buffer 8

h) error diffusion component = diffusion filter 9

As also discussed during the interview, the outputs (i.e., either integer, decimal, or both) can be seen to correspond as follows:

i) bit connection component: outputs both integer and decimal portions

ii) correction component: outputs both integer and decimal portions

iii) latch component: outputs decimal portion only

iv) quantization component: outputs integer portion only

v) inverse quantizing component: outputs integer portion only

vi) calculation component: output integer portion only

vii) buffer: output integer portion only

viii) error diffusion component: outputs integer and decimal portions, sign

Thus, as claimed, the bit connection component inputs the decimal portion latched by the latch for the previous corrected image data (pixel) and outputs bit-connected data for the target pixel. The bit-connected data (integer and decimal) is input to the correction component (2), along with a correction value output by the diffusion component. The correction component then outputs corrected image data to be quantized. However, prior to the quantization, the decimal portion of the corrected image data is split-off and latched by the latch so that only the integer portion is utilized in the quantization processing. This reduces the computational complexity and time for the quantization process than would otherwise be needed for quantization of both the integer and decimal portions. Additionally, less memory (buffer) capacity is used since the buffer stores the integer portion and not the decimal portion. The foregoing, while included in the claims, has nonetheless been made even clearer with regard to the splitting-off of the decimal portion and latching the split-off decimal portion before the quantization process such that only the integer portion is quantized. This feature is not seen to be taught by the cited art.

In this regard, the Examiner gave a preliminary indication that the splitting-off feature may be taught by Katayama, and the Examiner referred to Katayama teaching: "a quantization component that receives an integer portion of the corrected image data without receiving the decimal portion of the corrected image data of the target pixel (e.g., error-to-be-distributed computing means 904 for performing integral operations (with a decimal portion omitted) to obtain an error to be distributed to neighboring pixels from

signals output from the binarizing means 903 and the data adding means 902, column 19, lines 47-50)." It was pointed out to the Examiner that this portion of Katayama is believed to be different from the invention.

In this regard, it was noted that, in the invention, the decimal portion is split off before the quantization process and thus, the quantizer performs quantization based on the integer portion only. The split-off decimal portion is then added to the next pixel as part of the correction process. On the other hand, in Katayama, while an integer portion may be binarized, a decimal portion of the binarized result may be omitted after the binarization when computing the error for error diffusion. Therefore, the process of Katayama is different from the invention. The Examiner seemed to understand the foregoing, and stated that he would need to consult with his supervisor on this point.

Ishikawa and Nakano are not seen to remedy the foregoing deficiencies of Katayama. Ishikawa merely discloses that an output dot pattern is generated directly from a look up table (LUT). Nakano is merely seen to disclose a structure for a data driven device which includes an error diffusion computing unit having an error holding register and an error data memory. However, neither Ishikawa or Nakano are seen to teach anything that, when combined with Katayama, would have resulted in the features of a latch step of latching, by the latch component, a decimal portion of the corrected image data generated by the correction component of the target pixel by splitting-off, prior to performing quantization of the corrected image data, the decimal portion of the corrected image data from an integer portion of the corrected image data, output by the correction step, the split-off and latched decimal portion to be connected to the image data of the next pixel by the bit connection step, wherein the latch component does not latch the integer

portion of the corrected image data of the target pixel.

In view of the foregoing amendments and remarks, amended independent Claims 1, 20 and 39, as well as the claims dependent therefrom, are believed to be allowable over the applied art.

No other matters having been raised, the entire application is believed to be in condition for allowance and such action is respectfully requested at the Examiner's earliest convenience.

Applicant's undersigned attorney may be reached in our Costa Mesa, California office at (714) 540-8700. All correspondence should continue to be directed to our below-listed address.

Respectfully submitted,

/Edward Kmett/

Edward A. Kmett
Attorney for Applicant
Registration No.: 42,746

FITZPATRICK, CELLA, HARPER & SCINTO
1290 Avenue of the Americas
New York, New York 10104-3800
Facsimile: (212) 218-2200

FCHS_WS 5884311v1